

IN THE CLAIMS

Please add new claims as follows:

- 1 1. (original) A method for debugging a system comprising:
  - 2 1) coupling first signals to a re-writeable trace array, said trace array having  
3 M storage locations, said M storage locations having corresponding M storage addresses  
4 from a starting address to an ending address;
  - 5 2) generating a first event sequence signal in response to a first sequence of  
6 occurrences of a first event signal;
  - 7 3) starting, in response to said first event sequence signal, a process of  
8 storing states of said first signals sequentially in said trace array at locations beginning at  
9 said starting address and proceeding sequentially to said ending address, said process of  
10 storing states of said first signals wrapping back to said starting address when said ending  
11 address is exceeded;
  - 12 4) generating a second event sequence signal in response to a second  
13 sequence of occurrences of said first event signal;
  - 14 5) stopping said process of storing states of said first signals in said trace  
15 array in response to said second event sequence signal; and
  - 16 6) repeating steps 2) through 5) unless stopped by a second event signal.

- 1 2. (original) The method of claim 1, further comprising the step of:
  - 2 storing an event storage address in response to receipt of said first event  
3 sequence signal, said second event sequence signal or said second event signal, said  
4 event storage address corresponding to a storage address of sub-array K which is storing  
5 states of said first signals when said first event sequence signal, said second event  
6 sequence signal or said second event signal occurred.

- 1        3. (original) The method of claim 2, further comprising the steps of:  
2                reading stored states of said first signals from selected storage addresses of said  
3        trace array; and  
4                analyzing said stored states of said first signals to debug or analyze said system.
- 1        4. (original) The method of claim 3, wherein one of said stored event storage addresses  
2        is compared to a read storage address of said trace array during reading said stored states  
3        of said first signals, a comparison match of said stored event storage address to said read  
4        storage address corresponding to event or error states of said first signals.
- 1        5. (original) The method of claim 1, wherein said system comprises logic circuits in a  
2        very large scale integrated circuit (VLSI) chip.
- 1        6. (original) The method of claim 5, wherein said re-writeable trace array is included  
2        within said VLSI chip.
- 1        7. (original) The method of claim 1, wherein said first and second event signals are  
2        logic combinations of circuit states occurring within said system.
- 1        8. (original) The method of claim 1, wherein a storage address of said trace array,  
2        corresponding to said first event sequence signal, said second event sequence signal or  
3        said second event signal, is saved.
- 1        9. (original) The method of claim 1, wherein said first sequence of occurrences of said  
2        first event signal comprises a next sequential first event signal following a start signal.
- 1        10. (original) The method of claim 1, wherein said second sequence of occurrences of  
2        said first event signal comprises a next sequential first event signal following said first  
3        event sequence signal.

1 11. (original) The method of claim 9, wherein said second sequence of occurrences of  
2 said first event signal comprises a next sequential first event signal following said first  
3 event sequence signal .

1 12. (original) An apparatus for debugging a system comprising:

2 a coupling circuit operable to couple first signals to a re-writeable trace array, said  
3 trace array having N storage locations, said N storage locations having corresponding N  
4 storage addresses from a starting address to an ending address;

5 an event sequence circuit operable to generate a first event sequence signal in  
6 response to a first sequence of occurrence of a first event signal and a second event  
7 sequence signal in response to a second sequence of occurrence of said first event signal;

8 a store circuit operable to stores states of said first signals in said trace array by  
9 cyclically repeating the selection of said N storage addresses from a start storage address  
10 through an Nth storage address, said store circuit starting said store of said first signals in  
11 response to said first event sequence signal and stopping said store of said first signals in  
12 response to said second event sequence signal or a second event signal; and

13 a read circuit operable to read contents of said trace array at selected ones of said  
14 N storage addresses.

1 13. (original) The apparatus of claim 12, further comprising an address store circuit  
2 operable to store an event storage address in response to receipt of said first event  
3 sequence signal, said second event sequence signal or said second event signal, said  
4 event storage address corresponding to a storage address of said trace array which is  
5 storing states of said first signals when said first event sequence signal, said second event  
6 sequence signal or said second event signal occurred.

1 14. (original) The apparatus of claim 13, further comprising a compare circuit operable  
2 to compare one of said event storage addresses to a read storage address of said trace

3 array during reading said stored states of said first signals, a comparison match of said  
4 event storage address to said read storage address corresponding to event or error states  
5 of said first signals.

1 15. (original) The apparatus of claim 12, wherein said system comprises logic circuits in  
2 a very large scale integrated circuit (VLSI) chip.

1 16. (original) The apparatus of claim 15, wherein said re-writeable trace array is  
2 included within said VLSI chip.

1 17. (original) The apparatus of claim 12, wherein said first and second event signals are  
2 logic combinations of circuit states occurring within said system.

1 18. (original) The apparatus of claim 12, wherein contents of said trace array at selected  
2 addresses are read out and analyzed to debug or analyze said system.

1 19. (original) The apparatus of claim 12, wherein an address of said trace array,  
2 corresponding to said first event sequence signal, said second event sequence signal or  
3 said second event signal, is saved.

1 20. (original) The apparatus of claim 12, wherein said first sequence of occurrences of  
2 said first event signal comprises a next sequential first event signal following a start  
3 signal.

1 21. (original) The apparatus of claim 12, wherein said second sequence of occurrences  
2 of said first event signal comprises a next sequential first event signal following said first  
3 event sequence signal.

1 22. (original) The apparatus of claim 20, wherein said second sequence of occurrences  
2 of said first event signal comprises a next sequential first event signal following said first  
3 event sequence signal.

1 23. (original) A data processing system comprising:

2 a central processing unit (CPU);

3 random access memory (RAM);

4 read only memory (ROM);

5 an I/O adapter; and

6 a bus system coupling said CPU to said ROM, said RAM, wherein said CPU  
7 further comprises:

8 a very large scale integrated (VLSI) chip, said VLSI chip comprising a debugging  
9 system for debugging circuits within said chip said debugging system comprising;

10 a coupling circuit operable to couple first signals to a re-writeable trace array, said  
11 trace array having N storage locations, said N storage locations having corresponding N  
12 storage addresses from a starting address to an ending address;

13 an event sequence circuit operable to generate a first event sequence signal in  
14 response to a first sequence of occurrence of a first event signal and a second event  
15 sequence signal in response to a second sequence of occurrence of said first event signal;

16 a store circuit operable to stores states of said first signals in said trace array by  
17 cyclically repeating the selection of said N storage addresses from a start storage address  
18 through an Nth storage address, said store circuit starting said store of said first signals in  
19 response to said first event sequence signal and stopping said store of said first signals in  
20 response to said second event sequence signal or a second event signal; and

21 a read circuit operable to read contents of said trace array at selected ones of said  
22 N storage addresses.

1 24. (original) The data processing of claim 23, further comprising an address store  
2 circuit operable to store an event storage address in response to receipt of said first event  
3 sequence signal, said second event sequence signal or said second event signal, said

4 event storage address corresponding to a storage address of said trace array which is  
5 storing states of said first signals when said first event sequence signal, said second event  
6 sequence signal or said second event signal occurred.

1 25. (original) The data processing of claim 24, further comprising a compare circuit  
2 operable to compare one of said event storage addresses to a read storage address of said  
3 trace array during reading said stored states of said first signals, a comparison match of  
4 said event storage address to said read storage address corresponding to event or error  
5 states of said first signals.

1 26. (original) The data processing of claim 23, wherein said system comprises logic  
2 circuits in a very large scale integrated circuit (VLSI) chip.

1 27. (original) The data processing of claim 26, wherein said re-writeable trace array is  
2 included within said VLSI chip.

1 28. (original) The data processing of claim 23, wherein said first and second event  
2 signals are logic combinations of circuit states occurring within said system.

1 29. (original) The data processing of claim 23, wherein contents of said trace array at  
2 selected addresses are read out and analyzed to debug or analyze said system.

1 30. (original) The data processing of claim 23, wherein an address of said trace array,  
2 corresponding to said first event sequence signal, said second event sequence signal or  
3 said second event signal, is saved.

1 31. (original) The data processing of claim 23, wherein said first sequence of  
2 occurrences of said first event signal comprises a next sequential first event signal  
3 following a start signal.

1 32. (original) The data processing of claim 23, wherein said second sequence of  
2 occurrences of said first event signal comprises a next sequential first event signal  
3 following said first event sequence signal.

1 33. (original) The data processing of claim 32, wherein said second sequence of  
2 occurrences of said first event signal comprises a next sequential first event signal  
3 following said first event sequence signal.

1 34. (new) A method for debugging a system comprising:

2 1) coupling first signals to a re-writeable trace array having M storage locations  
3 with corresponding M storage addresses from a starting address to an ending address;

4 2) generating a start/stop signal on an occurrence of an event sequence;

5 3) starting a process of recording states of said first signals in the trace array in a  
6 present storage address in said M storage addresses in response to said start/stop signal  
7 by enabling a write to said trace array and incrementing said present storage address  
8 proceeding sequentially to said ending address, wherein said present storage address  
9 wraps back to said starting address when said ending address is exceeded;

10 4) stopping the process of recording states of said first signals in said trace array  
11 at said present storage address in response to said start/stop signal generated by a next  
12 occurrence of said event sequence following said occurrence of said event sequence  
13 starting said process of recording states of said first signals; and

14 5) repeating steps 2) through 4) until stopped by an error signal different from  
15 said start/stop signal.

1 35. (new) The method of claim 34, further comprising the step of:

2 storing said present storage address in response to said start/stop signal or said  
3 error signal.

1 36. (original) The method of claim 35, further comprising the steps of:

2           enabling a read of said trace array and reading recorded states of said first signals  
3           from selected storage addresses of said trace array following an occurrence of said error  
4           signal; and  
5           analyzing said recorded states of said first signals to debug or analyze said  
6           system.